1GHzPLL

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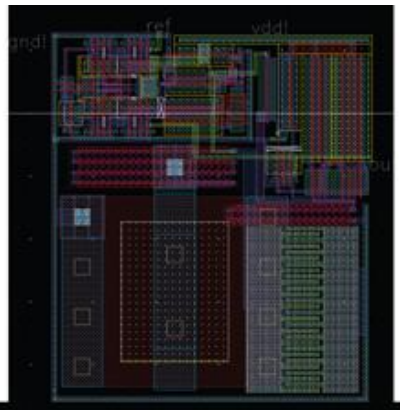

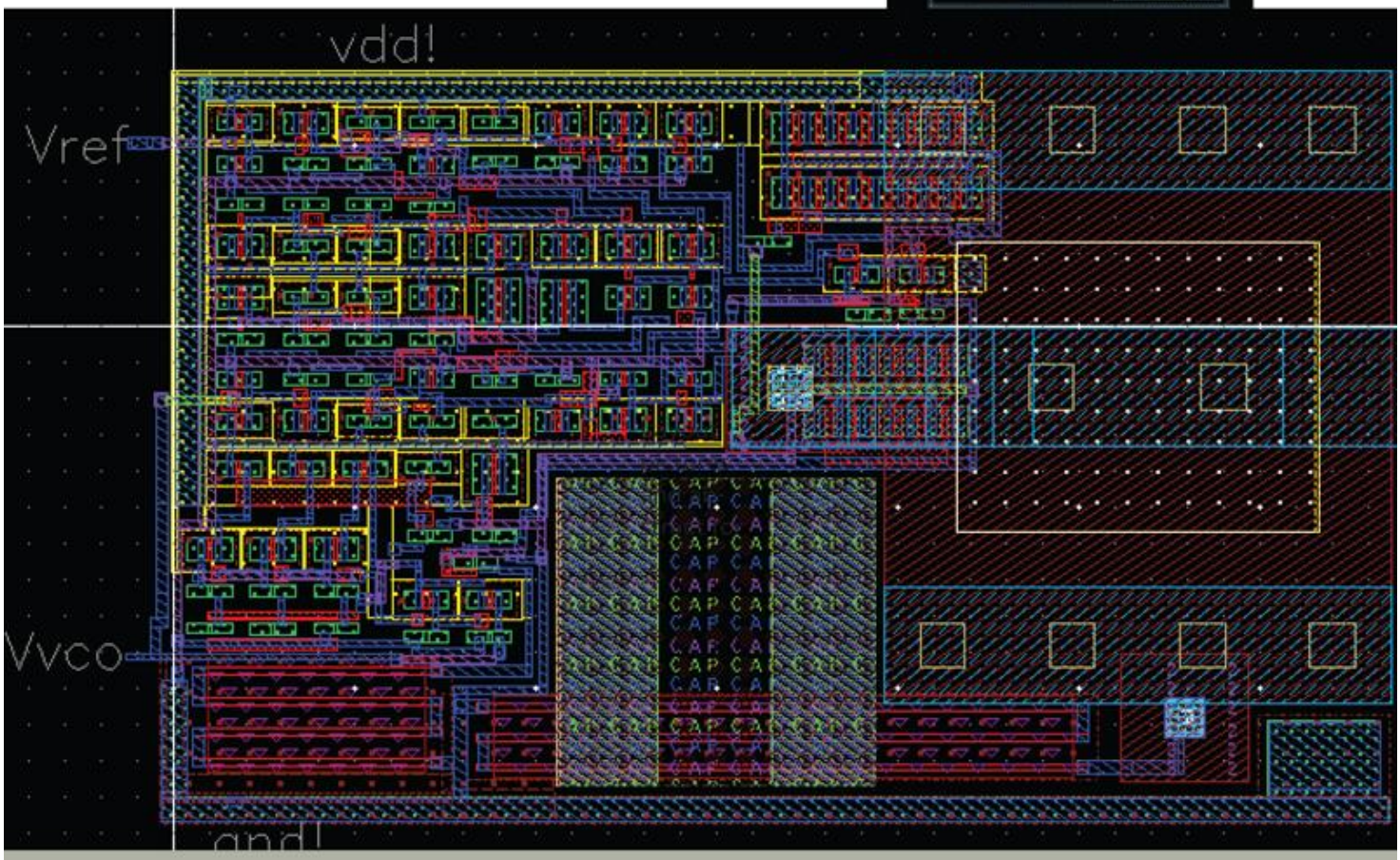

The goal in designing a Phase Locked Loop (PLL) is to track the precise frequency and phase of a reference signal, and then reproduce the signal at the output of the device using a feedback system. At a higher level of abstraction, the Phase Frequency Detector PFD finds the difference between the phase of the output and the reference, and outputs a pulse corresponding to either a phase lag or phase lead. These pulses control switches in the next functional block, the charge pump/loop filter (CP/LF), which charges/discharges the node that controls the final block, the Voltage Controlled Oscillator (VCO). This type of oscillator changes its frequency of oscillation depending on the control voltage applied to it, thus allowing the system to make adjustments to a phase lag/lead by increasing/decreasing the output frequency such that the phase locks with the reference. PLL's have applications in computer clock synchronization, FM demodulation, and frequency synthesis.

Two designs were implemented in schematic and layout. Both layouts are being fabricated by MOSIS, and lab tests will be conducted to quantify performance metrics.

WORK SPACE SHOWCASE
THE COOPER UNION ANNUAL STUDENT EXHIBITION
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